

FINAL DRAFT

AEC - QXXX-XXX - REV-

~~April 25~~ August 15, 2007

Automotive Electronics Council  
Component Technical Committee

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ATTACHMENT XX

AEC - QXXX-XXX - REV-

PB-FREE TEST REQUIREMENTS

Proposed Draft  
(subject to change)

# Automotive Electronics Council

## Component Technical Committee

### Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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**Automotive Electronics Council**  
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This document contains a set of tests and defines the minimum requirements for qualification of lead free (Pb-free) metallurgy for components to be used in any automotive electronics application. For a component to be considered Pb-free compatible, its properties, including but not limited to plating materials and package configuration, must be compatible with Pb-free manufacturing processes. Use of this document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all customers using a component qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document.

**1.1 Purpose**

The purpose of this specification is to determine that a component is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application. The science of whisker growth, including growth models and accelerated test methods, is not fully understood at the time of release of this standard. Further, the existence of tin whiskers over time does not ensure component or system failure. The environmental tests specified in this document for whisker growth evaluation require conditions of temperature, humidity and temperature cycling which are currently believed to best exacerbate whisker growth in Sn-plated leads and terminations. The user and supplier need to consider the applicable risks when using components with Sn-plated leads in sensitive applications.

**1.2 Reference Documents**

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

**1.2.1 Military**

MIL-STD-202 Test Method Standard – Electronic and Electrical Component Parts

**1.2.2 Industrial****1.2.2.1 JEDEC**

JESD201 Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes

JESD22-A104 Temperature Cycling

JESD22-A111 Evaluation Procedure for Determining Capability to Bottom Side Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices

JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

JESD22-A121 Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes

JESD22-B102 Solderability

JP002 Current Tin Whiskers Theory and Mitigation Practices Guideline

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### 1.2.2.2 IPC/JEDEC

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires  
J-STD-020 Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices

## 1.3 Terms and Definitions

**1.3.1 Lead Free (Pb-free) Plating Finish:** A component plating finish is considered Pb-free if the following requirements are met:

- a. < 0.1% (1000PPM) concentration of Pb by weight in homogeneous materials.
- b. No intentional addition of Pb as part of the component plating finish manufacturing process.
- c. Is compliant to typical Pb-free board assembly process and material(s) (as defined in this document).
- d. Complies with the latest version of the Global Automotive Declarable Substance List (GADSL). Refer to GADSL ([www.gadsl.org](http://www.gadsl.org)) for detailed requirements and exemptions.

### 1.3.2 Preferred Pb-Free Finishes

Due to the risk of Sn whiskers, all finishes containing no Sn are preferred, such as NiPd or NiPdAu. However, solderability performance may indicate a preference of Sn plating over NiPd or NiPdAu. Therefore, careful consideration must be given to the plating finish material and the intended component manufacturing process.

A whisker mitigation practice is required ~~W~~when Sn-based finishes are used, unless otherwise agreed between user and supplier on a case-by-case basis. ~~Preferred mitigation practices, as defined in Refer to Section 5 of JP002 for information regarding mitigation practices, include the following:~~

- ~~a. Use a Ni barrier underlayer; other materials (e.g., Ag, etc.) may be used provided the requirements of this document are met~~
- ~~b. Sn plating thickness >7um~~
- ~~c. Postbake anneal of 1 hour at 150°C, performed within 24 hours of plating~~

~~**Note:** Actual material thickness values may vary depending on plating process and component type. Data must be provided by the Supplier to demonstrate that actual material thickness values will meet the requirements stated in this specification.~~

### 1.3.3 Restricted Pb-Free Finishes

**1.3.3.1 Tin-Bismuth (SnBi) alloy finishes are not acceptable for use in SnPb solder processes** due to the formation of a low-melting point ternary eutectic compound (SnPbBi). Use of SnBi alloy finishes in SnPb solder processes requires user approval and must meet the requirements stated in this specification.

**1.3.3.2 Plated Tin-Copper (SnCu) alloy finishes are not acceptable for use in any solder process** due to enhanced whisker formation and growth resulting from the introduction of Copper. Use of SnCu alloy finishes requires user approval and must meet the requirements stated in this specification.

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### 2. EQUIPMENT

Not Applicable

### 3. QUALIFICATION TESTS

When a component involves Pb-free and/or Pb-free compatible materials, certain tests (as defined in this document) must be performed and resulting data submitted for review before the component can be approved for use. These tests are in addition to all electrical/mechanical testing required in the applicable part specification and include solderability, resistance to solder heat (if applicable), moisture sensitivity (MSL), and Sn whisker testing (see Figure 1 and sections 3.1 to 3.4). Where applicable, tests should include exposure to and/or use of standard SnPb (e.g., Sn60/Pb40, Sn63/Pb37, Sn25/Pb75, etc.) and Pb-free (SAC305 or similar Pb-free alloy with liquidus of 217°C to 227°C) solder to examine and confirm forward and backward assembly compatibility of the Pb-free components. **The user must approve any deviation from the test requirements defined herein.**

#### 3.1 Solderability

All plated component terminations and/or surfaces shall be tested for solderability as defined herein, and according to usage per the applicable [AEC-QXXX test specification qualification document](#) (e.g., AEC-Q100, AEC-Q101, [and/or AEC-Q200](#)) [and corresponding solderability test specification](#), (e.g., MIL-STD-202, JESD22-B102, and/or J-STD-002). Solderability testing must include preconditioning as defined and required in the applicable [AEC-QXXX test specification qualification document](#)(s). All exceptions to the applicable test method(s) must be noted in the part specification.

##### 3.1.1 Solderability - Dip and Look Test

Solderability testing using the Dip and Look test method shall be performed per the applicable test specification (e.g., J-STD-002 Test A, JESD22-B102 Method 1, etc.). Dip and Look testing shall include use of both SnPb and Pb-free solder alloys [and temperatures](#) as defined in the applicable test specification, ~~and shall be performed at the solder test temperatures defined in Section 3.1.3.~~

##### 3.1.2 Solderability - Surface Mount Process Simulation Test

Solderability testing using the Surface Mount Process Simulation test method shall be performed per the applicable test specification (e.g., J-STD-002 Test S, JESD22-B102 Method 2, etc.). [Unless otherwise agreed upon between user and supplier, the nominal stencil thickness, solder alloy, and reflow parameters \(i.e., temperature and time\) shall be as defined in the applicable test specification.](#) ~~Surface Mount Process Simulation testing shall consist of the following:-~~

- ~~a. Use of stencil(s) as defined by the user~~
- ~~b. Use of both SnPb and Pb-free solder alloys as defined by the user~~
- ~~c. Solder test temperatures as defined in Section 3.1.3~~

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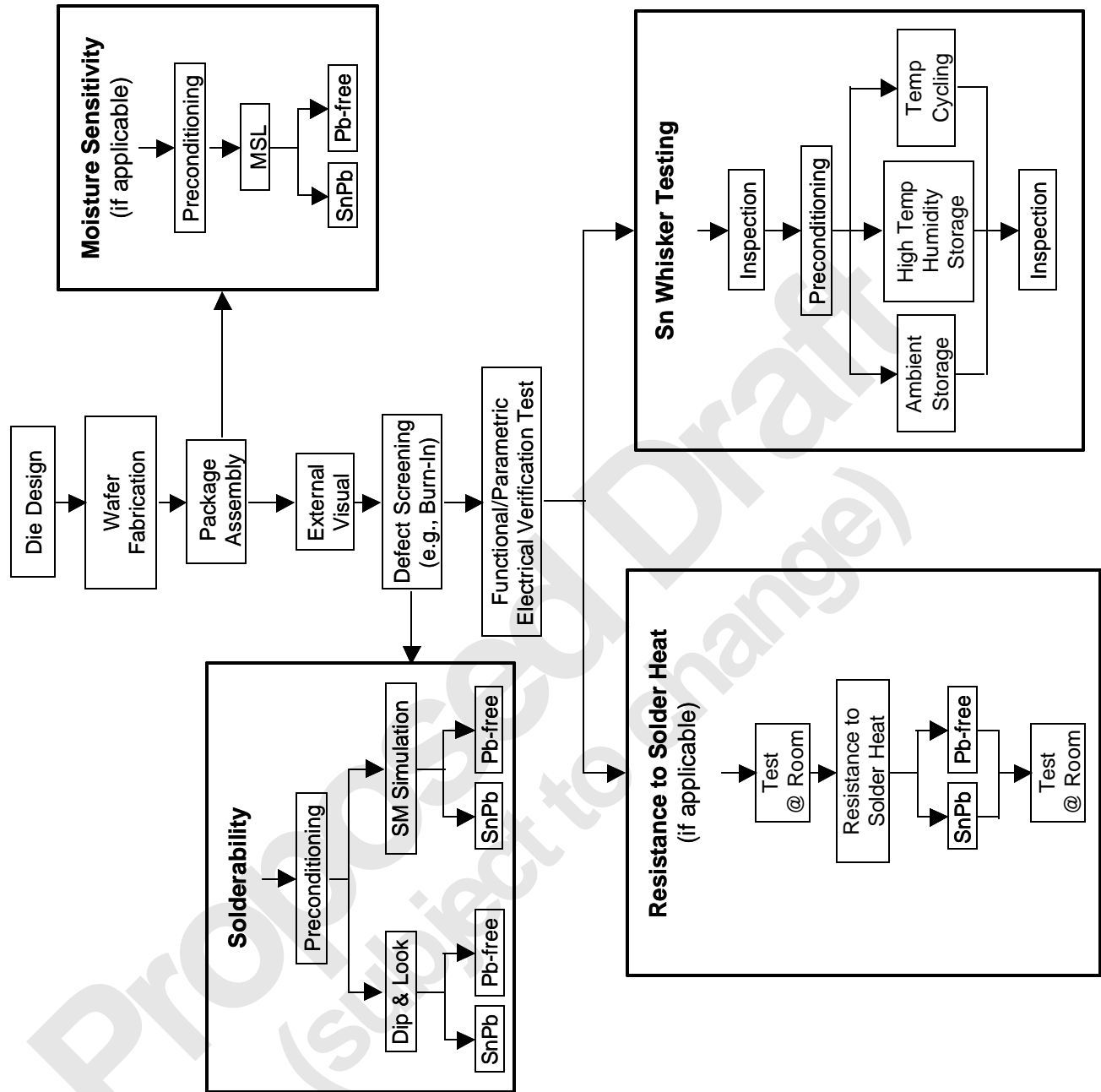


Figure 1: Typical Pb-Free Qualification Test Flow (in addition to to all electrical/mechanical testing required in the applicable part specification)

\* Note: Actual qualification test flow shall be per the applicable AEC-QXXX [test specification qualification document](#)(s).

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**3.1.3 Solderability Test Temperatures**

~~To demonstrate forward (Pb-free) and backward (SnPb) solder process compatibility, solderability testing shall be performed at the test temperatures shown in Table 1. Additional test temperatures may be required per agreement between user and supplier on a case-by-case basis.~~

**Table 1: Required Solderability Test Temperatures**

Solder Process	Solder Test Temperature
SnPb (backward compatibility)	215°C
Pb-free (forward compatibility)	245°C

**3.1.4 Solderability Accept Criteria**

~~Solder coverage area shall exhibit at least a 95% continuous, smooth new solder coating. Voids, pinholes, porosity, non-wetting, or dewetting in any area shall not exceed 5% of the total solderability area.~~

**3.1.53 Wetting Balance Testing**

In the event that component solderability issues are encountered, the Wetting Balance Test method can be a valuable investigation technique. If required, Wetting Balance testing shall be performed according to the procedure defined in J-STD-002 Test E (or equivalent). Additional requirements may be applicable per agreement between user and supplier on a case-by-case basis.

**3.2 Resistance to Solder Heat**

Resistance to Solder Heat testing must be performed per the applicable AEC-XXX Qqualification ~~Specification document~~ (e.g., [AEC-Q100](#), [AEC-Q101](#), ~~and/or AEC-Q200, etc.~~). If no requirement exists, then testing as defined in this section is required. Components representative of device families shall be tested for resistance to solder heat per the applicable test specification (e.g., MIL-STD-202, JESD22-B106 - Through-Hole, and/or JESD22-A111 - Surface Mount). All exceptions to the applicable test specification(s) must be noted in the part specification.

**3.2.1 Through-Hole Components**

Resistance to solder heat testing of thru-hole components shall be performed per the applicable test specification (e.g., JESD22-B106 and/or MIL-STD-202 - Method 210). Following testing per the applicable test specification(s), samples must pass all part specification requirements and shall exhibit no evidence of mechanical damage.

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**3.2.2 Surface Mount Components (only applies if attached using bottom-side wave solder process)**

It is strongly recommended that SMT components not be attached by bottom-side wave solder processes. Resistance to solder heat testing of surface mount components (if applicable) shall be performed per the applicable test method (e.g., JESD22-A111 and/or MIL-STD-202 - Method 210). Testing performed per JESD22-A111 shall use dry samples (no moisture soak) and use dual wave simulation as defined in Table 1 of JESD22-A111. Following testing per the applicable test method, samples must pass all part specification requirements and shall exhibit no evidence of mechanical damage.

**3.3 Moisture Sensitivity**

Components representative of device families shall be tested to determine moisture sensitivity classification per the applicable [AEC-QXXX qualification document \(e.g., AEC-Q100, AEC-Q101, and/or AEC-Q200\)](#) and corresponding test specification (e.g., JSTD-020 MSL-Reflow, and/or JESD22-A113 Preconditioning), for both SnPb and Pb-free solder profiles. If applicable, both SnPb and Pb-free moisture sensitivity levels and temperatures shall be identified (e.g., MSL-1/235°C, MSL-3/260°C, etc.). ~~Any drop in existing MSL requires further investigation and~~ the user shall be notified [of any drop in existing MSL classification](#) to determine impact. All exceptions must be noted in the part specification.

**3.3.1** Moisture preconditioning requirement for tantalum capacitors is currently under development within various industry standards organizations (e.g., EIA P2.5 Tantalum Committee). Pending a final proposal from these organizations, all moisture preconditioning requirements for tantalum capacitors shall be per AEC-Q200.

**3.3.2** Surface Mount components to be attached using bottom-side wave solder process shall be tested to determine moisture sensitivity classification per the applicable test specification (e.g., JSTD-020 MSL - Reflow, JESD22-A111 MSL-Wave Solder, and/or JESD22-A113 Preconditioning). Testing shall use the preconditioning levels defined in JSTD-020 and follow the moisture classification procedure defined in Table 1 and section 5 of JESD22-A111. If applicable, both SnPb and Pb-free moisture sensitivity levels and temperatures shall be identified (e.g., MSL-1/235°C, MSL-3/260°C, etc.)

**3.4 Tin (Sn) Whisker Acceptance Testing**

**3.4.1** Whisker acceptance testing shall be compliant to JESD201, with additional requirements as defined herein.

**3.4.2** Sn whisker testing is mandatory for each component family using a Sn-based finish material. Nickel-palladium (NiPd) or nickel-palladium-gold (NiPdAu) finishes do not require tin whisker testing.

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### 3.4.3 Areas of Concern and Caution (when performing JESD201 acceptance testing)

#### 3.4.3.1 Initial Sample Inspection

Following the plating process and prior to sample preconditioning, all sample components shall be inspected at a magnification level (e.g., 50X to 150X) capable of identifying the presence of whisker-like features (e.g., dendrites) that are a function of the finish and not whiskers. Refer to JESD22-A121 for inspection equipment requirements. All identified features shall be recorded and photographed for reference and comparison during final inspection.

#### 3.4.3.2 Handling Precaution

Care must be taken during handling of test samples to avoid possible damage or detachment of whiskers due to excessive vibration or physical contact with component finish material. The procedures defined in Section 6 of JESD22-A121 should be followed to avoid sample contamination and minimize possible whisker damage/detachment.

#### 3.4.3.3 Sample Preconditioning

Test samples must be preconditioned according to JESD201 and JESD22-A121. Preconditioning levels include:

- a. No preconditioning (control)
- b. Room temperature storage (minimum of 4 weeks); \* **Note**: Only required for samples without under-plating or post bake mitigation
- c. SnPb solder reflow profile (see JESD22-A121 for profile specification)
- d. Pb-free reflow profile (see JESD22-A121 for profile specification)

#### 3.4.3.4 Whisker Acceptance Test – Temperature & Humidity Storage

The temperature and humidity storage conditions are close to the condensation point. Water condensing in the test chamber (e.g., on walls, ceiling, etc.) or component plating finish material can result in corrosion that may affect whisker test results. Care must be taken to avoid condensation (refer to Section 4.2 of JESD22-A121 for details and cautions).

### 3.4.4 Additional Requirements (addendum to JESD201)

#### 3.4.4.1 Test Samples

Samples shall be representative of actual product and package family using the proposed Pb-free finish, including any trim and form operations that occur after the plating process. Definition of package family requires agreement between user and supplier on a case-by-case basis.

#### 3.4.4.2 Sample Preconditioning - Board Mounting

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Due to the addition of solder alloy material and its interaction with the Pb-free plating finish material, use of a solder alloy or attaching test samples to a printed circuit board using a soldering operation is prohibited. Deviation requires agreement between user and supplier on a case-by-case basis.

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### 3.4.4.3 Validation of Whisker Acceptance Test Conditions

The test conditions defined in JESD201 have been shown to generate whiskers. If whiskers are not detected over the required test duration for either temperature cycling or high temperature and humidity storage test conditions, data must be provided to validate the test conditions used. The temperature/humidity storage test condition (30°C ±2°C and 60% ±3% RH) is exempt from this requirement.

#### 3.4.4.4 Optional Requirements per User Request

The following information may be required by the user. Any deviation or non-conformance to the optional requirements as stated herein must be approved by the user.

##### 3.4.4.4.1 Demonstration of Whisker Growth Saturation

If whisker growth is observed during the required High Temperature/Humidity Storage storage test conditions (Temperature/Humidity Storage and High Temperature/Humidity Storage), whisker testing and inspection shall continue for an additional 500 hours if the data meets the following criteria:

- a. A single non-zero whisker measurement at the 4000 hour readpoint interval (no whiskers detected at previous readpoint intervals).
- b. Non-zero whisker measurements at the last two readpoint intervals (e.g., 3000 hour and 4000 hour) indicating a growth rate greater than or equal to 10µm the extrapolated saturation line.

##### 3.4.4.4.1 Extrapolated Saturation Line

The extrapolated saturation line is determined by connecting a line between the 3000 hour readpoint whisker length value and a data point of 40µm at 6000 hours. If the 4000 hour whisker length value is less than the extrapolated saturation line, then whisker growth is assumed to be saturated and no additional testing is required. If the 4000 hour whisker length value is greater than or equal to the extrapolated saturation line, then whisker growth is assumed to be active and an additional 500 hours of testing is required.

##### 3.4.4.4.2 Acceptance Criteria for Demonstration of Whisker Growth Saturation

A component will be defined as meeting the demonstration of whisker growth saturation requirement if all samples meet the following criteria:

- a. Less than or equal to 10µm increase in maximum whisker length between the 4000 hour readpoint value and the additional 500 hour readpoint (i.e., 4500 hour) value.
- b. Class level 2 requirements, as defined in JESD201.

### 3.4.5 Acceptance Criteria

A component will be defined as passing Sn whisker acceptance testing if all test samples meet the following criteria established by the user. This criteria may include, but is not limited to, the following:

- a. Class level 2 requirements, as defined in JESD201.

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- b. Deviation from Class level 2 requires agreement between user and supplier on a case-by-case basis.

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#### 3.5 Reporting of Results

Upon completion of the required testing defined herein, a report of the tests performed and detailed results must be submitted to the user. This report should include, but is not limited to:

- a. Plating Finish Details
  - Component type, package, base metal, underlayer (if used), finish material(s)
  - Whisker mitigation used
  - Material thickness values
- b. Sample Details
  - Plating lot date
  - Package configuration (e.g., package dimensions, lead pitch, pin count, lead form, etc.)
  - Preconditioning used (e.g., solderability, MSL, Sn Whisker, etc.)
  - Sample sizes
- c. Test Details
  - Testing performed (e.g., solderability, MSL, Sn Whisker, etc.)
  - Documentation of solder alloy and/or solder profile/temperature used (e.g., SnPb, Pb-free, etc.)
  - Whisker test conditions (e.g., intervals, durations, sample sizes, etc.)
  - Exceptions to any tests performed (e.g., test conditions, corrosion, etc.)
- d. Test Results
  - Acceptance criteria (for all tests performed)
  - Actual test data for all tests performed
  - Maximum whisker length measured at each test interval
  - Whisker saturation (if applicable)

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**Revision History**

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	TBD	Initial Release

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