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Re: IPC/EIA/JEDEC Joint Standard Solderability Test Specification Experiment – IPC-003

Mark Kwoka - Intersil

We've finished solderability evaluations of the components you provided for the IPC / EIA / JEDEC Joint Standard Solderability Test Specification Designed Experiment, Before solderability testing we characterized the surface finish thickness on the PDIP and Cerdip component leads using X-Ray Fluorescence (XRF). A Dip-&-Look solderability test was performed according to the directions you provided. This correspondence serves to document our evaluations and provide the solderability test results for inclusion into the designed experiment evaluation.

A photograph showing the component types provided is presented in Figure 1. The documentation you provided indicated the surface finishes on the components to be:

- ?? 8 I/O SOIC – Ni/Pd
- ?? 14 I/O PDIP (DC9237) - 300?in of hot dipped tin-lead (Sn63/Pb37) solder
- ?? 14 I/O Cerdip – 100% electroplated tin (Sn)
- ?? 44 I/O MQFP (DC9531) – electroplated Sn80/Pb20 solder
- ?? 2 I/O Chip Caps – Sn plated

Before performing Dip-&-Look solderability tests, the surface finish on the components was characterized using XRF. The XRF spectrum presented in Figure 2a confirms that the surface finish on the PDIP leads is SnPb. The Figure 2b spectrum also confirms that the surface finish on the Cerdip components is Sn. However, the spectrum of the ceramic chip capacitor terminations presented in Figure 2c indicates that the surface finish on the chip caps is silver (Ag) rather than Sn. The surface finish on the 8 I/O SOIC and 44 I/O MQFP components was measured previously and reported in Lucent Technologies Report IPC-002.

The photographs of PDIP leads presented in Figure 3a and 3b show what appears to be bright, shiny, hot dipped leads. The photographs presented in Figure 3c and 3b show

| IPC/EIA/JEDEC Joint Standard Solderability Test Specification Design Experiment | | | | |
|---|------------------|-------|------------------|-------|
| J-STD-002A Dip - & - Look Test Method A Category 1 (No Steam Age) | | | | |
| Component Type Lead Count and Surface Finish | ROLO 235C 3 Sec. | | ROL1 235C 3 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 0 / 10 | 0 / 5 | 1 / 10 | 1 / 5 |
| SOIC 8 I/O PdNi | 2 / 80 | 2 / 5 | 0 / 80 | 0 / 5 |
| MQFP 44 I/O SnPb | 3 / 110 | 1 / 5 | 0 / 110 | 0 / 5 |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| | | | | |
| Component Type Lead Count and Surface Finish | ROLO 235C 5 Sec. | | ROL1 235C 5 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 0 / 10 | 0 / 5 | 0 / 10 | 0 / 5 |
| SOIC 8 I/O PdNi | 0 / 80 | 0 / 5 | 0 / 80 | 0 / 5 |
| MQFP 44 I/O SnPb | 0 / 110 | 0 / 5 | 0 / 110 | 0 / 5 |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| | | | | |
| Component Type Lead Count and Surface Finish | ROLO 240C 3 Sec. | | ROL1 240C 3 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 0 / 10 | 0 / 5 | | |
| SOIC 8 I/O PdNi | 0 / 80 | 0 / 5 | | |
| MQFP 44 I/O SnPb | 0 / 110 | 0 / 5 | | |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | | |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | | |
| | | | | |
| Component Type Lead Count and Surface Finish | ROLO 240C 5 Sec. | | ROL1 240C 5 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 0 / 10 | 0 / 5 | | |
| SOIC 8 I/O PdNi | 0 / 80 | 0 / 5 | | |
| MQFP 44 I/O SnPb | 0 / 110 | 0 / 5 | | |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | | |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | | |
| | | | | |
| Component Type Lead Count and Surface Finish | ROLO 245C 3 Sec. | | ROL1 245C 3 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 1 / 10 | 1 / 5 | 0 / 10 | 0 / 5 |
| SOIC 8 I/O PdNi | 0 / 80 | 0 / 5 | 0 / 80 | 0 / 5 |
| MQFP 44 I/O SnPb | 0 / 110 | 0 / 5 | 0 / 110 | 0 / 5 |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| | | | | |
| Component Type Lead Count and Surface Finish | ROLO 245C 5 Sec. | | ROL1 245C 5 Sec. | |
| | Leads | Units | Leads | Units |
| Chip Cap 2 I/O Ag | 0 / 10 | 0 / 5 | 0 / 10 | 0 / 5 |
| SOIC 8 I/O PdNi | 0 / 80 | 0 / 5 | 0 / 80 | 0 / 5 |
| MQFP 44 I/O SnPb | 0 / 110 | 0 / 5 | 0 / 110 | 0 / 5 |
| PDIP 14 I/O SnPb | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |
| CERDIP 14 I/O Sn | 0 / 70 | 0 / 5 | 0 / 70 | 0 / 5 |

Key: # Rejected / # Inspected

Table 1. Dip-&-Look Solderability Test Results

PDIP leads after being Dip-&-Look solderability tested. There is little if any discernible difference between the as received and Dip-&-Look tested leads.

XRF measurements of the surface finish thickness and composition on the outside surface of the PDIP leads were made in the area that would be wave soldered to printed wiring board plated through holes. Frequency distributions of the XRF measurements are presented in Figures 4 and 5. The surface finish on the leads averages 300 microinches of 63% Sn. Even though these components are 8 years old they appear bright and shiny and look like they should be extremely solderable, which the Dip-&-Look test results confirmed.

Photographs presented in Figure 6 show the electroplated Sn surface of CERP leads. The XRF spectrum presented in Figure 2b confirmed Sn as the surface finish. A frequency distribution of the Sn plating thickness measurements is presented in Figure 7. The Sn is extremely thick, averaging over 1000 microinches.

Each of the components was Dip-&-Look solderability tested using the solder temperature, immersion time, and flux specified in your request. Our inspection results from the Dip-&-Look solderability testing are presented in Table 1. We also inspected the components for solder bridges. The only leads that bridged during solderability testing were those of the 44 I/O, 0.8 mm pitch MQFP. The number of bridged gaps between gull wing leads over the number of possible gaps is presented in Table 2.

| Solder Temperature (Degree C) | # of Bridged Gaps Between Leads / # of Gaps | | | |
|-------------------------------|---|-----------|-----------|-----------|
| | ROLO | | ROL1 | |
| | 3 Seconds | 5 Seconds | 3 Seconds | 5 Seconds |
| 235 | 59 / 100 | 89 / 100 | 52 / 100 | 49 / 100 |
| 240 | 71 / 100 | 56 / 100 | | |
| 245 | 49 / 100 | 42 / 100 | 42 / 100 | 29 / 200 |

Table 2. 44 I/O MQFP bridged lead gaps

The photographs in Figure 8 show all but one of the solderability defects detected. As shown in Figure 1c, one end of a chip capacitor tested using ROL1 flux, 235°C, 3-second immersion failed to wet above the immersion depth. Figure 2d shows one lead of an 8 I/O SOIC tested using ROLO, 235°C, 3 second immersion, that failed to wet above the immersion depth. Figure 8e shows the two leads of a 44 I/O MQFP that did not wet and one lead that failed to wet above the immersion depth.

During the Dip-&-Look solderability testing of the chip capacitors we noticed that the solder meniscus wet to a higher level when using ROL1 than ROLO flux. Photographs comparing the capacitor terminal wetting for each flux type is presented in Figure 9.

If you have any questions concerning our solderability evaluations or require the components for others to inspect please let us know.

George M. Wenger

Electronic Email Copy to:

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J. (Jack) K. Dorey – Lucent -PR
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Leslie A. Guth – Lucent -PR
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Brian J. Toleno – ACI

Dennis Fritz - MacDermid

Carol Handwerker - NIST

Dave Hillman - Rockwell

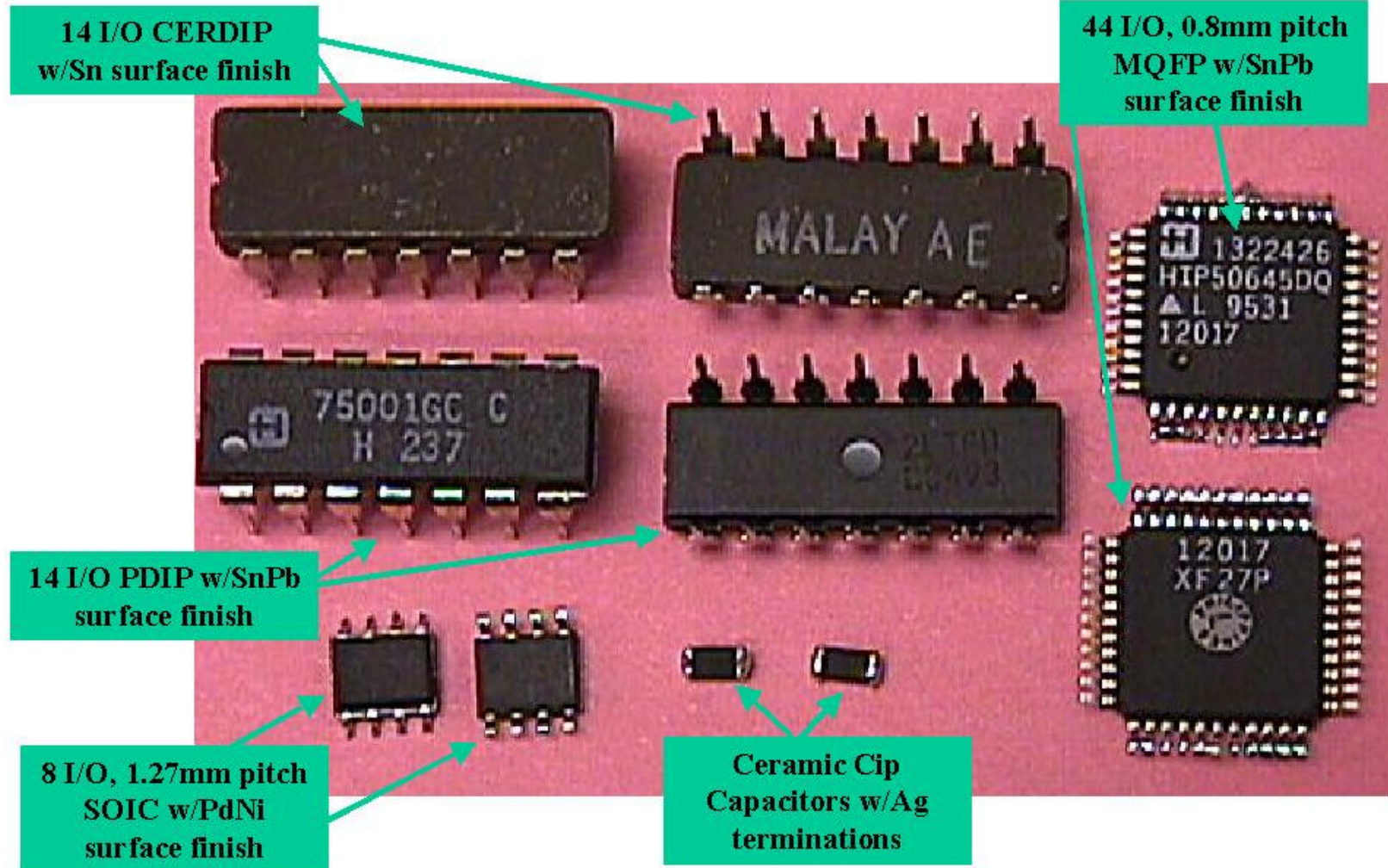


FIGURE 1.
**COMPONENTS USED FOR IPC / EIA / JEDEC JOINT STANDARD
SOLDERABILITY TEST SPECIFICATION DESIGNED EXPERIMENT**

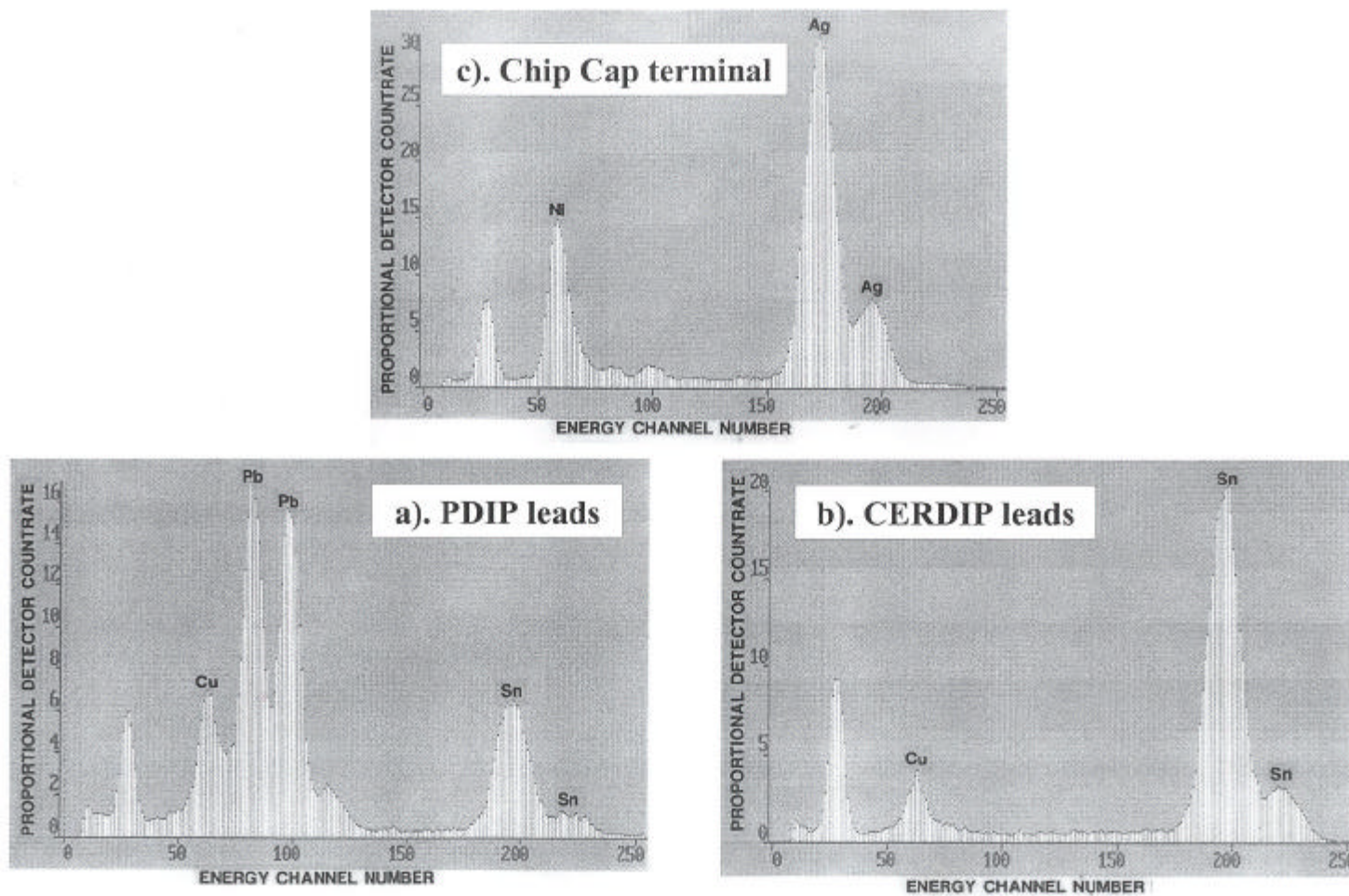


FIGURE 2.
XRF SPECTRA OF COMPONENT LEADS AND TERMINALS

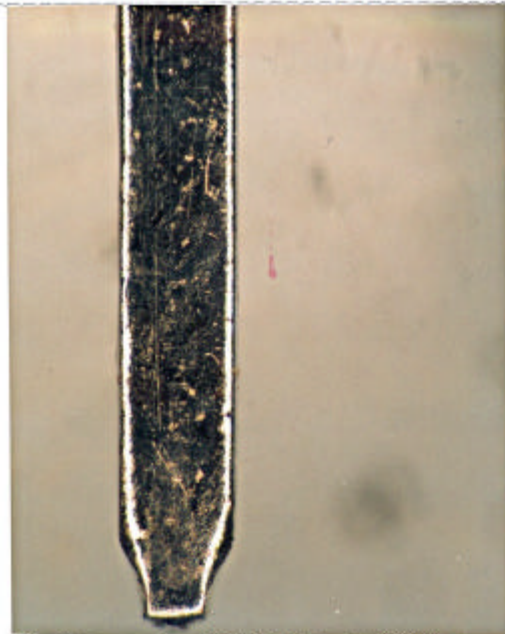
**FIGURE 3.
PHOTOS OF 14 I/O PDIP LEADS**



a). As-received PDIP leads (16x)



c). Lead after Dip-&-Look (16x)



b). As-received PDIP lead (48x)



d). Lead after Dip-&-Look (48x)

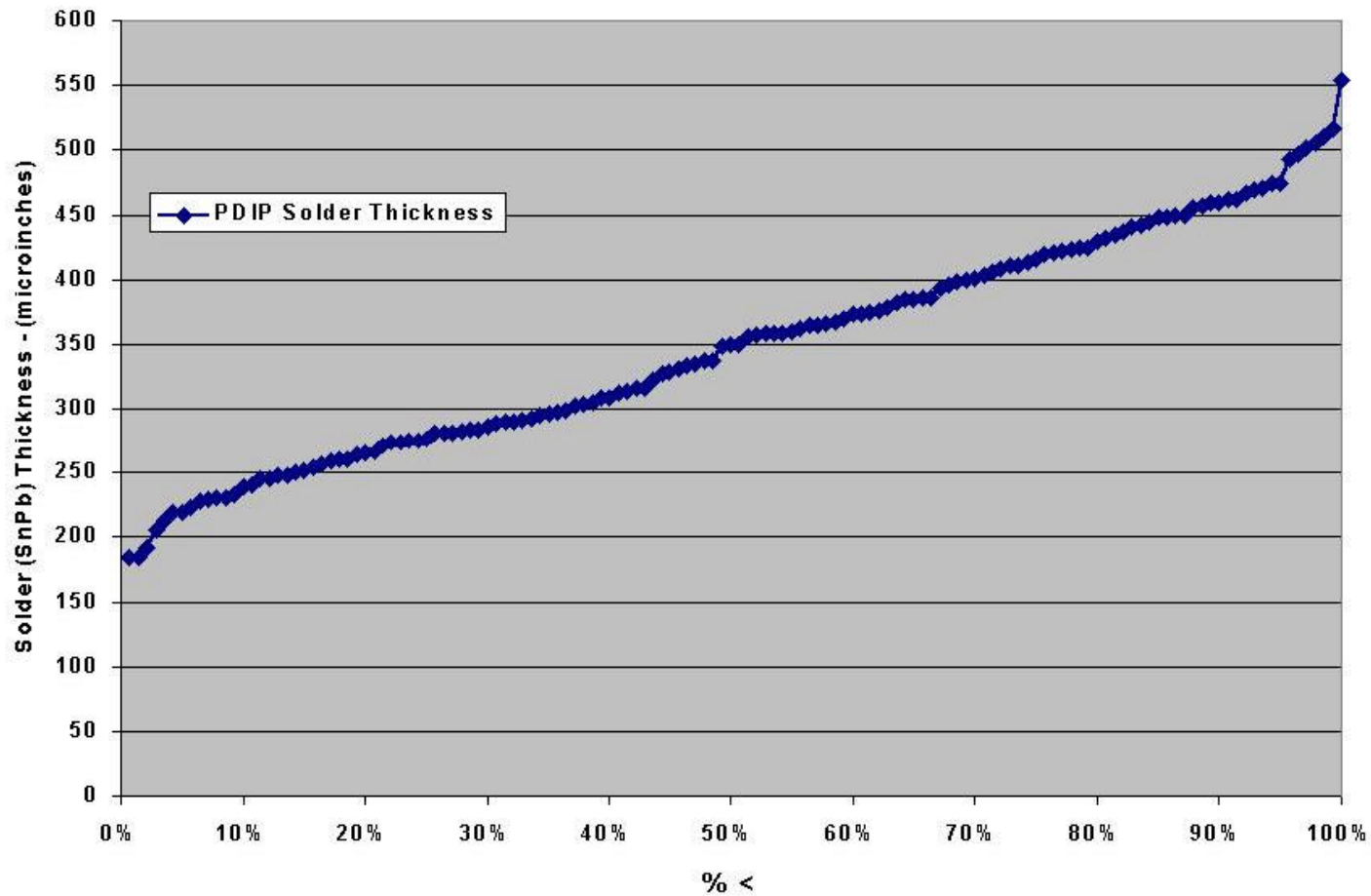


FIGURE 4.
FREQUENCY DISTRIBUTION OF 14 I/O PDIP XRF MEASURED
SnPb SOLDER THICKNESS

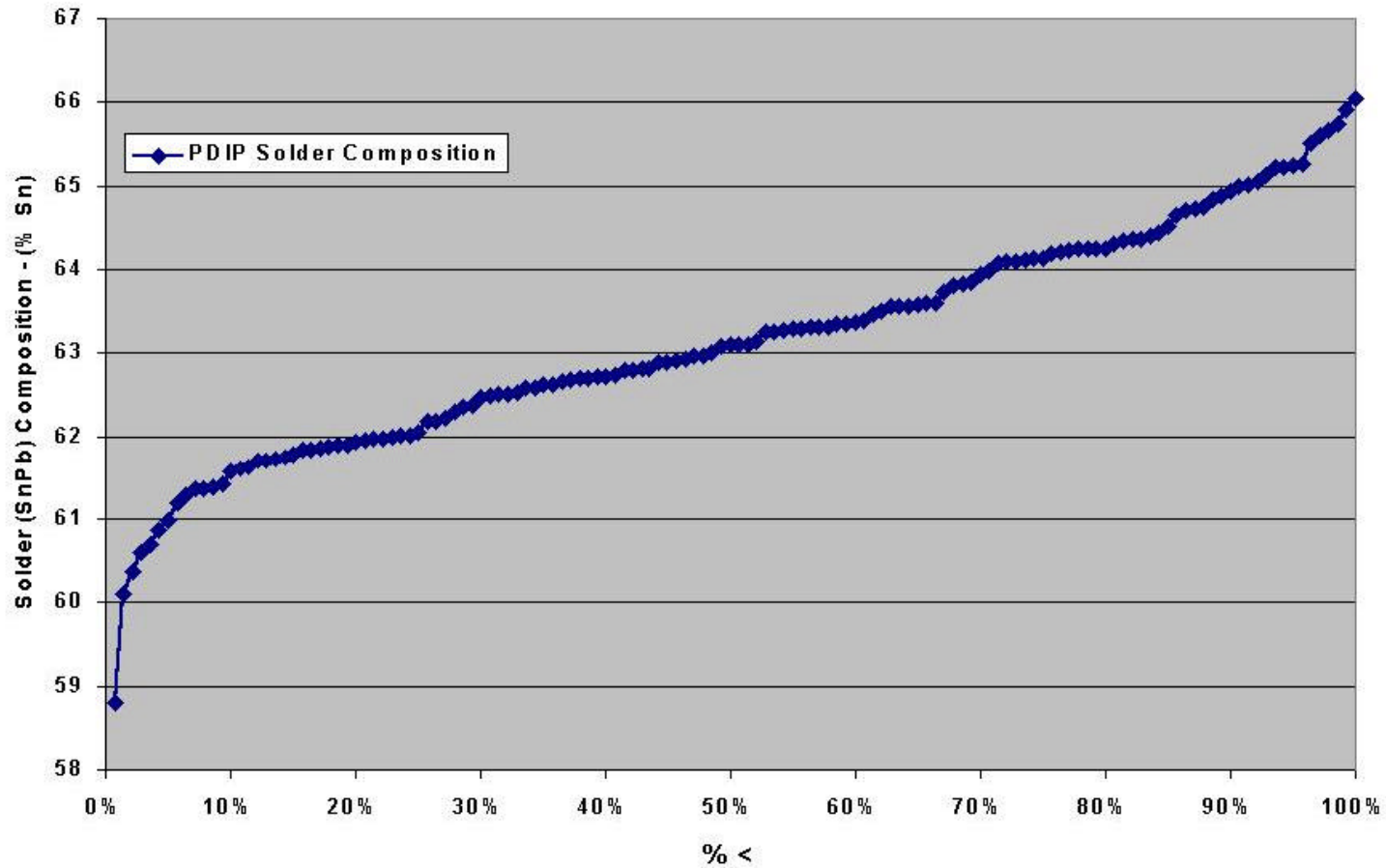


FIGURE 5.
FREQUENCY DISTRIBUTION OF 14 I/O PDIP XRF MEASURED
SnPb SOLDER COMPOSITION

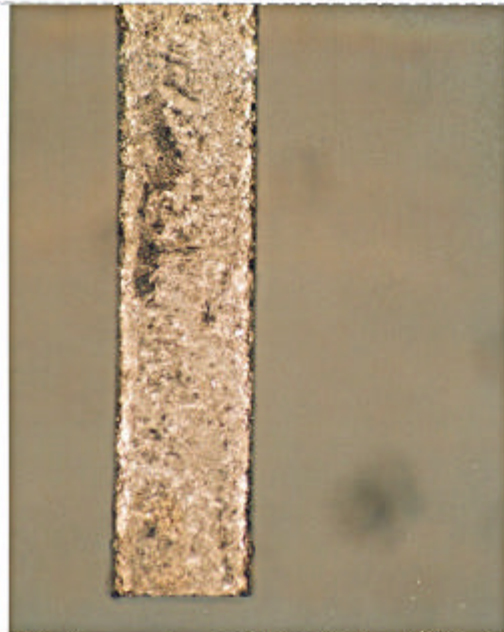
FIGURE 6.
PHOTOS OF 14 I/O CERDIP LEADS



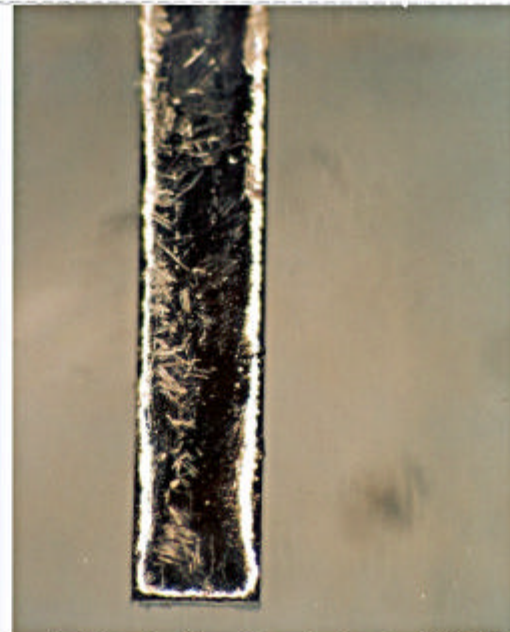
a). As-received CERDIP leads (16x)



c). Lead after Dip-&-Look (16x)



b). As-received CERDIP lead (48x)



d). Lead after Dip-&-Look (48x)

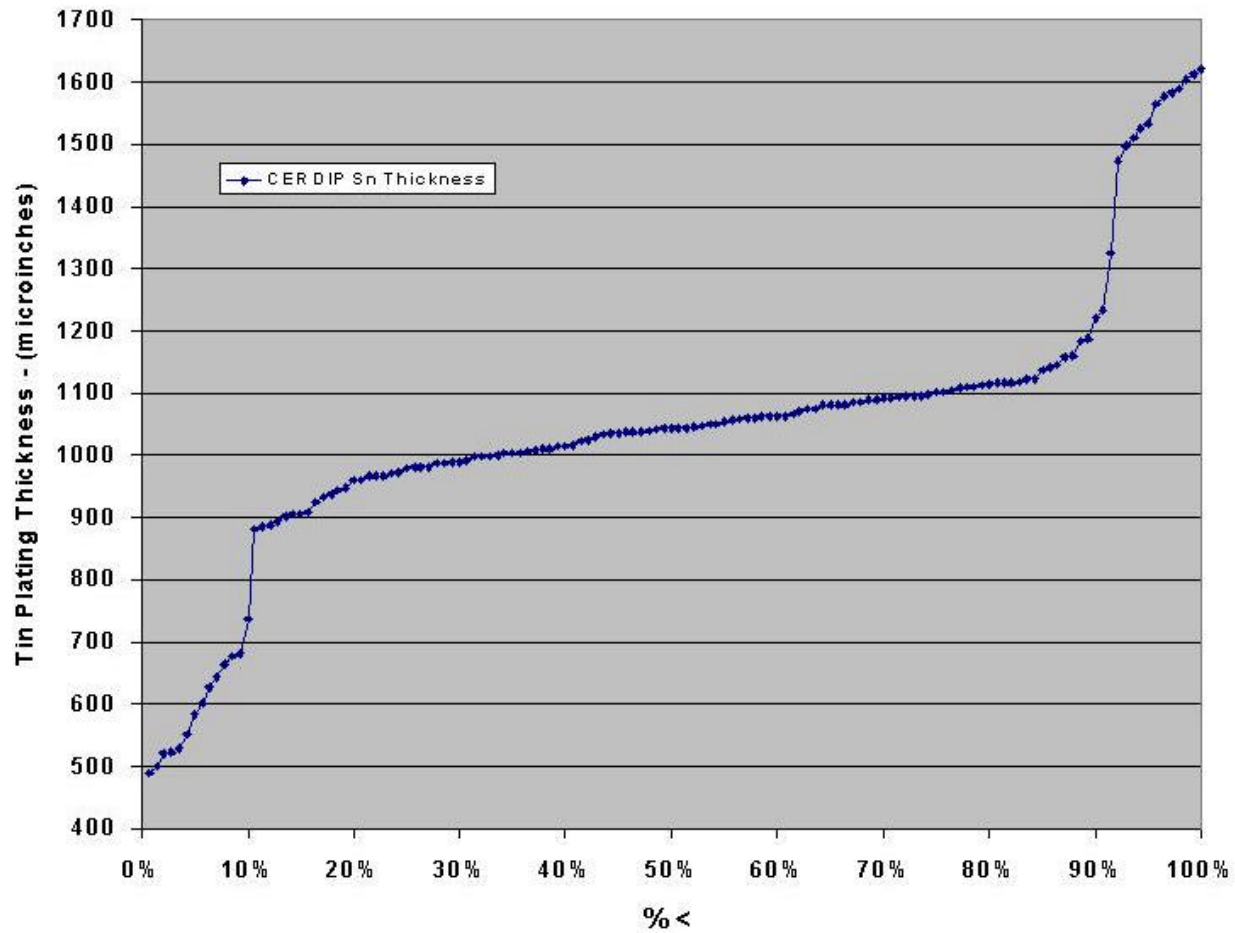


FIGURE 7.
FREQUENCY DISTRIBUTION OF 14 I/O CERDIP XRF
MEASURED Sn PLATING THICKNESS

FIGURE 8.
DIP-&-LOOK SOLDERABILITY TEST DEFECTS
(Red Line Indicates Depth of Solder Immersion)

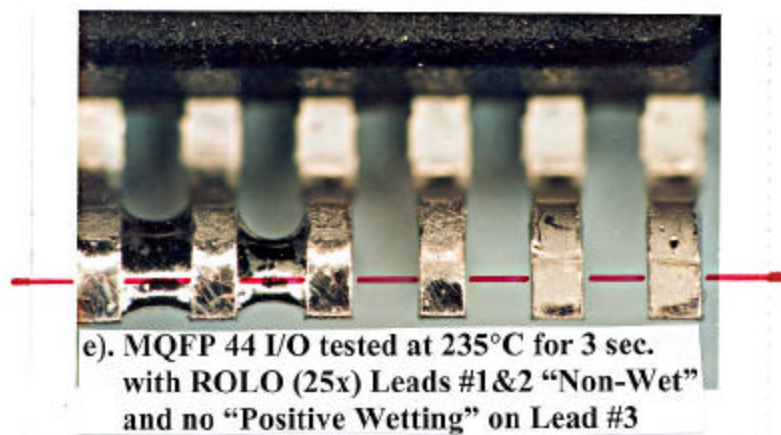
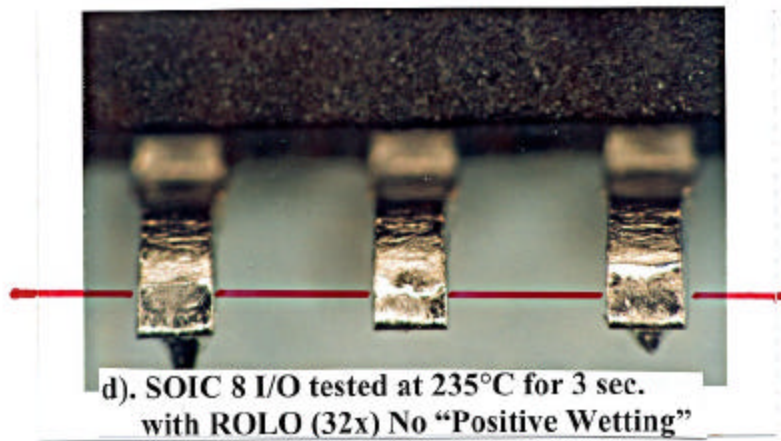
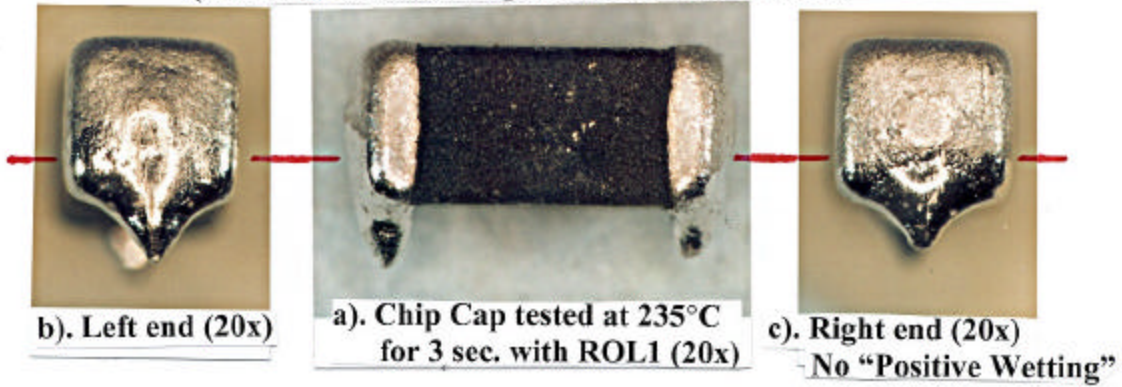


FIGURE 9.
COMPARISON OF ROLO AND ROL1 FLUX
DIP-&-LOOK SOLDERABILITY TEST ON
CHIP CAPACITORS

(Red Line Indicates Depth of Solder Immersion)

